32-bit ARM® Cortex™-M3 Microcontroller,up to 256KB Flash and 32KB SRAM with 1 MSPS ADC, USART, UART, SPI, I²C, I²S, MCTM, GPTM, BFTM, PDMA, SCI, CRC, EBI and USB2.0 FS

HT32F1656/HT32F1655 Series DataSheet

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1 General Description

The Holtek HT32F1656/1655 devices are high performance, low power consumption 32-bit microcontrollers based around an ARM® Cortex™-M3 processor core. The Cortex™-M3 is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and includes advanced debug support.

The devices operate at a frequency of up to 72 MHz with a Flash accelerator to obtain maximum efficiency. They provide up to 256 KB of embedded Flash memory for code/data storage and 32 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I^2C, USART, UART, SPI, I^2S, PDMA, GPTM, MCTM, SCI, EBI, CRC-16/32, USB2.0 FS, SW-DP (Serial Wire Debug Port), etc., are also implemented in the devices. Several power saving modes provide the flexibility for maximum optimisation between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the devices are suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control, fingerprint recognition and so on.

2 Features

Core

- 32-bit ARM® Cortex™-M3 processor core
- Up to 72 MHz operating frequency
- 1.25 DMIPS/MHz (Dhrystone 2.1)
- Single-cycle multiplication and hardware division
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex™-M3 processor is a general-purpose 32-bit processor core especially suitable for products requiring high performance and low power consumption microcontrollers. It offers many special features such as a Thumb-2 instruction set, hardware divider, low latency interrupt respond time, atomic bit-banding access and multiple buses for simultaneous accesses. The Cortex™-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets.

On-chip Memory

- Up to 256 KB on-chip Flash memory for instruction/data and option storage
- 32 KB on-chip SRAM
- Supports multiple boot modes

The ARM® Cortex™-M3 processor is structured using Harvard architecture which uses a separate bus structure to fetch instructions and load/store data. The instruction code and data are both located in the same memory address space but in different address ranges. The maximum address range of the Cortex™-M3 is 4 GB due to its 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex™-M3 processor to reduce the software complexity of repeated implementation for different device vendors. However, some regions are used by the ARM® Cortex™-M3 system peripherals. Refer to the ARM® Cortex™-M3 Technical Reference Manual for more information. Figure 2 shows the memory map of the HT32F1656/55 series of devices, including Code, SRAM, peripheral, and other pre-defined regions.

Flash Memory Controller

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit

- Supply supervisor:
  - Power-on Reset - POR
  - Brown-out Detector - BOD
  - Programmable Low Voltage Detector - LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8MHz RC oscillator trimmed to ±2% accuracy at 3.3V operating voltage and 25°C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers and clock gating circuitry. The clocks of the AHB, APB and Cortex™-M3 are derived from the system clock (CK_SYS) which can come from the HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source. The maximum operating frequency of the system core clock (CK_AHB) can be up to 72 MHz.

Power Management

- Single 3.3 V power supply: 2.7 V to 3.6 V
- Integrated 1.8 V LDO regulator for core and peripheral power supply
- V_{BAT} battery power supply for RTC and backup registers
- Three power domains: 3.3 V, 1.8 V and Backup
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate - 1 μs at 56 MHz, 1.17 μs at 72 MHz
- Up to 16 external analog input channels
- Supply voltage range: 2.7 V ~ 3.6 V
- Conversion range: V_{REF+} ~ V_{REF-}

A 12-bit multi-channel ADC is integrated in the device. There are up to 16 multiplexed channels, which include external channels on which the external analog signals can be measured, and 2 internal channels. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

Analog Operational Amplifier/Comparator

- Two Operational Amplifiers or Comparator functions which are software configurable
- Supply voltage range: 2.7 V ~ 3.6 V

Two Operational Amplifiers/Comparators (OPA/CMP) are implemented within the devices. They can be configured either as Operational Amplifiers or as Analog Comparators. When configured as comparators, they are capable of generating interrupts to the NVIC.

I/O Ports

- Up to 80 GPIOs
- Port A, B, C, D, E are mapped as 16 external interrupts - EXTI
- Almost all I/O pins are 5 V-tolerant except for pins shared with analog inputs

There are up to 80 General Purpose I/O pins, GPIO, named from PA0~PA15 to PE0~PE15 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximise flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins.

The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

PWM Generation and Capture Timers – GPTM

- Two 16-bit General-Purpose Timers - GPTM
- Up to 4-channel with PWM, Compare Output or Input Capture function for each GPTM
- External trigger input

The General Purpose Timers, known as GPTM0 and GPTM1, consist of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation, or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Motor Control Timer – MCTM

- Two 16-bit up, down, up/down auto-reload counters
- 16-bit programmable prescaler allowing division of the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with edge aligned and centre-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Encoder interface controller with two inputs using quadrature decoder
- Supports 3-phase motor control and hall sensor interface
- Brake input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of a single 16-bit up/down counter; four 16-bit CCRs (Capture/Compare Registers), single one 16-bit counter-reload register (CRR), single 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM supports an Encoder interface controller to an incremental encoder with two inputs. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

Basic Function Timer – BFTM

- Two 32-bit compare/match count-up counters - no I/O control features
- One shot mode - counting stops after a match condition
- Repetitive mode - restart counter after a match condition

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer

- 12-bit down counter with 3-bit prescaler
- Interrupt or reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT counter value register, a WDT delta value register, interrupt related circuits, WDT operation control circuitry and a WDT protection mechanism. The Watchdog Timer can be operated in an interrupt mode or a reset mode. The Watchdog Timer will generate an interrupt or a reset when the counter counts down and reaches a zero value. If the software does not reload the counter value before a Watchdog Timer underflow occurs, an interrupt or a reset will be generated when the counter underflows. In addition, an interrupt or reset is also generated if the software reloads the counter when the counter value is greater than or equal to the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Real Time Clock

- 32-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC for short, includes an APB interface, a 32-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the V_{DD18} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{DD18} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provide an arbitration function and clock synchronisation
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I²C Module is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 1. 100 kHz in the Standard mode, 2. 400 kHz in the Fast mode and 3. 1 MHz in the Fast mode plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I²C module also has an arbitration detect function and clock synchronisation to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave mode
- Frequency of up to 36 MHz for master mode and 24MHz for slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud rate up to 4.5 MHz and synchronous operating rate up to 9 MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- Auto hardware flow control mode - RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 16 x 9 bits for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a 16-byte transmitter FIFO, (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate up to 4.5 MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- FIFO Depth: 16 x 9 bits for both receiver and transmitter

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The UART module includes a 16-byte transmitter FIFO, (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO). The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Smart Card Interface – SCI

- Supports ISO 7816-3 standard
- Character mode
- Single transmit buffer and single receive buffer
- 11-bit ETU (elementary time unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and checking
- Automatic character retry on parity error detection in transmission and reception modes

The Smart Card Interface is compatible with the ISO 7816-3 standard. This interface includes Card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform all the necessary Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

Inter-IC Sound – I²S

- Master or slave mode
- Mono and stereo
- I²S-justified, Left-justified, and Right-justified mode
- 8/16/24/32-bit sample size with 32-bit channel extended
- 8 x 32-bit Tx & Rx FIFO with PDMA supported
- 8-bit Fractional Clock Divider with rate control

The I²S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADCs or DACs. The I²S supports a variety of data formats. In addition to the stereo I²S-justified, Left-justified and Right-justified modes, there are mono PCM modes with 8/16/24/32-bit sample size. When the I²S operates in the master mode, then when using the fractional divider, it can provide an accurate sampling frequency output and support the rate control function and fine-tuning of the output frequency to avoid system problems caused by the cumulative frequency error between different devices.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16}+X^{15}+X^{2}+1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16}+X^{12}+X^{5}+1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as input and generates a 16- or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 8 channels with trigger source grouping
- 8-/16-/32-bit width data transfer
- Supports Address increment, decrement or fixed mode
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source: ADC, SPI, USART, UART, I²C, I²S, EBI, GPTM, MCTM, SCI and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to join each data movement operation.

External Bus Interface – EBI

- Programmable interface for various memory types
- Translate the AHB transactions into the appropriate external device protocol
- Memory bank regions and independent chip select control for each memory bank
- Programmable timings to support a wide range of devices
- Includes page read mode
- Automatic translation when the AHB transaction width and external memory interface width is different
- Write buffer to decrease the stalling of the AHB write burst transaction
- Supports multiplexed and non-multiplexed address and data line configurations
- Up to 25 address lines
- Up to 16-bit data bus width

The external bus interface is able to access external parallel interface devices such as SRAM, Flash and LCD modules. The interface is memory mapped into the internal address map of the Cortex-M3. The data and address lines can be multiplexed in order to reduce the number of pins required to connect to the external devices. Tthe read/write timing of the bus can be adjusted to meet the timing specification of the external devices. Note the interface only supports asynchronous 8 or 16-bit bus interface.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 full-speed (12Mbps) specification
- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1,024 bytes EP-SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte SRAM is used as the endpoint buffer. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimise the overall system complexity and cost. The USB functional block also contains the resume and suspend feature to meet the requirements of low-power consumption.

Debug Support

- Serial Wire Debug Port - SW-DP
- 6 instruction comparators and 2 literal comparators for hardware breakpoint or code / literal patches
- 4 comparators for hardware watchpoints
- 1-bit asynchronous trace (TRACESWO)

Package and Operation Temperature

- 48/64/100-pin LQFP package
- Operation temperature range: -40°C to +85°C

3 Overview

Device Information

Table 1. HT32F1656/1655 Series Features and Peripheral List

Peripherals		HT32F1656	HT32F1655
Main Flash (KB)		255	128
Option Bytes Flash		1	1
SRAM (KB)		32	32
Timers	MCTM	2	
	GPTM	2	
	BFTM	2	
	RTC	1	
	WDT	1	
Communication	USB	1	
	SPI	2	
	USART	2	
	UART	2	
	I^2C	2	
	I^2S	1	
	SCI	1	
EBI		1	
CRC-16/32		1	
EXTI		16	
12-bit ADC Number of channels		1	
		16 Channels	
OPA/Comparator		2	
GPIO		Up to 80	
CPU frequency		Up to 72 MHz	
Operating voltage		2.7V ~ 3.6V	
Operating temperature		-40°C ~ +85°C	
Packages		48/64/100-pin LQFP	

Block Diagram

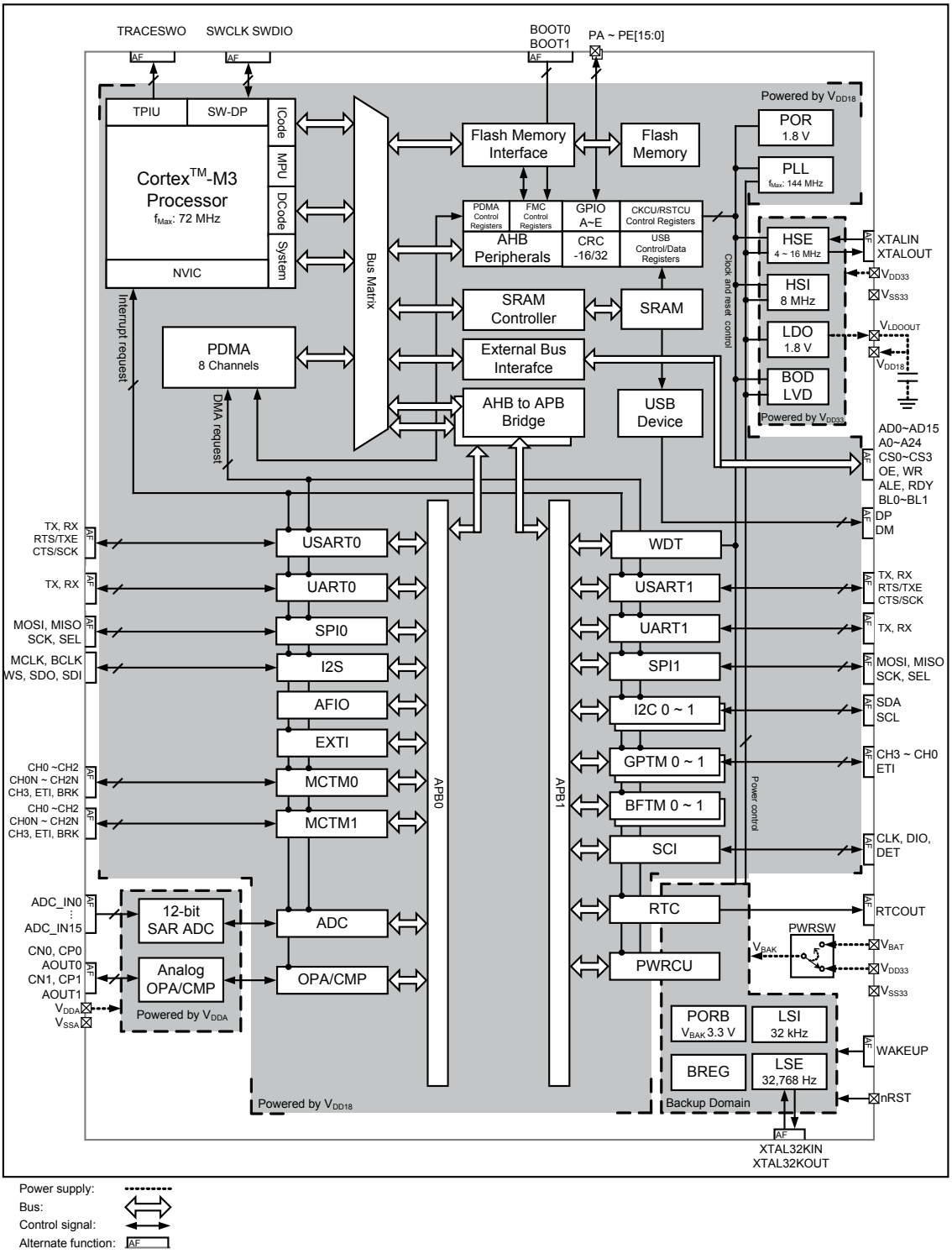


Figure 1. HT32F1656/1655 Block Diagram

Memory Map

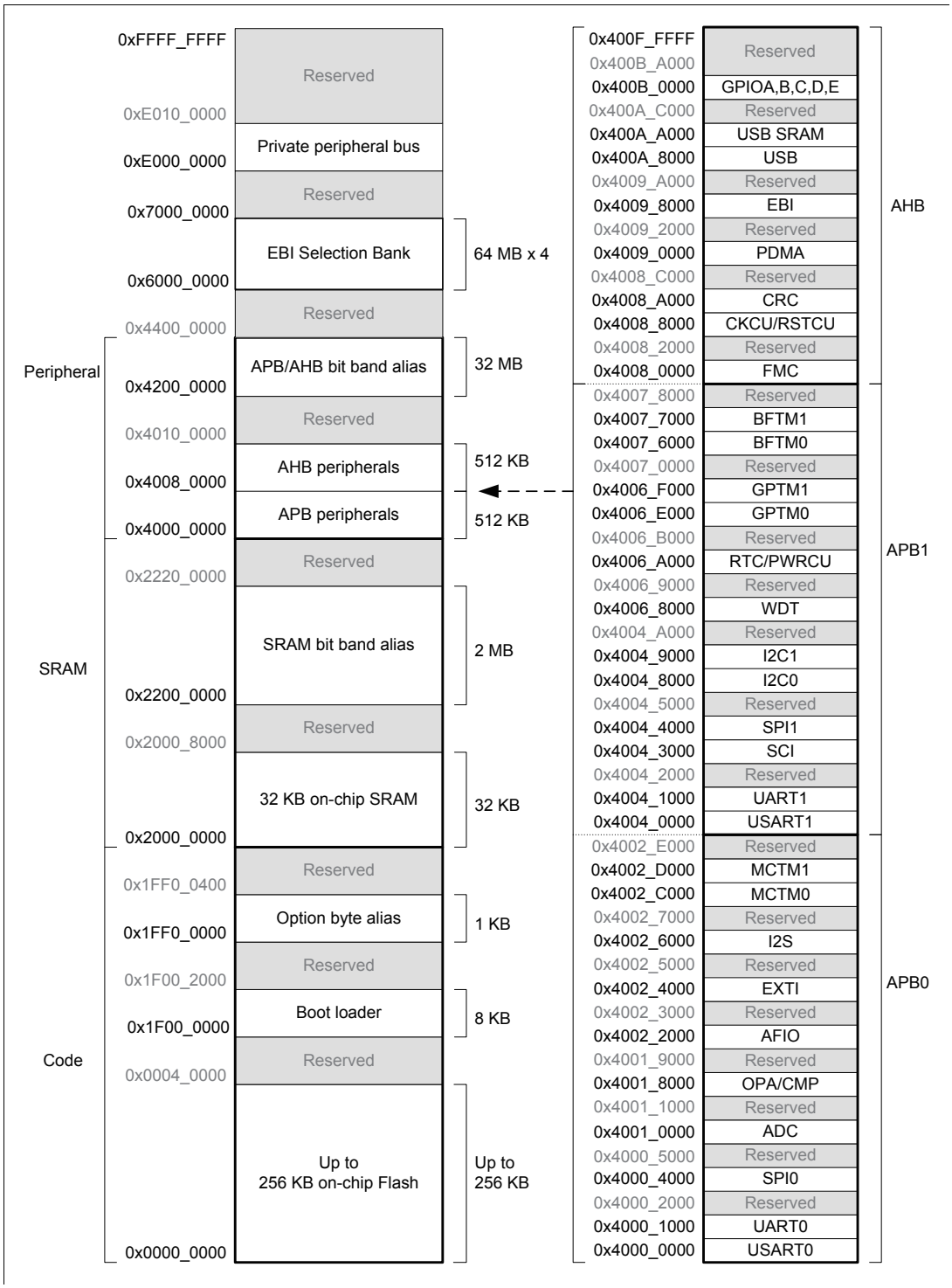


Figure 2. HT32F1656/1655 Memory Map

Clock Structure

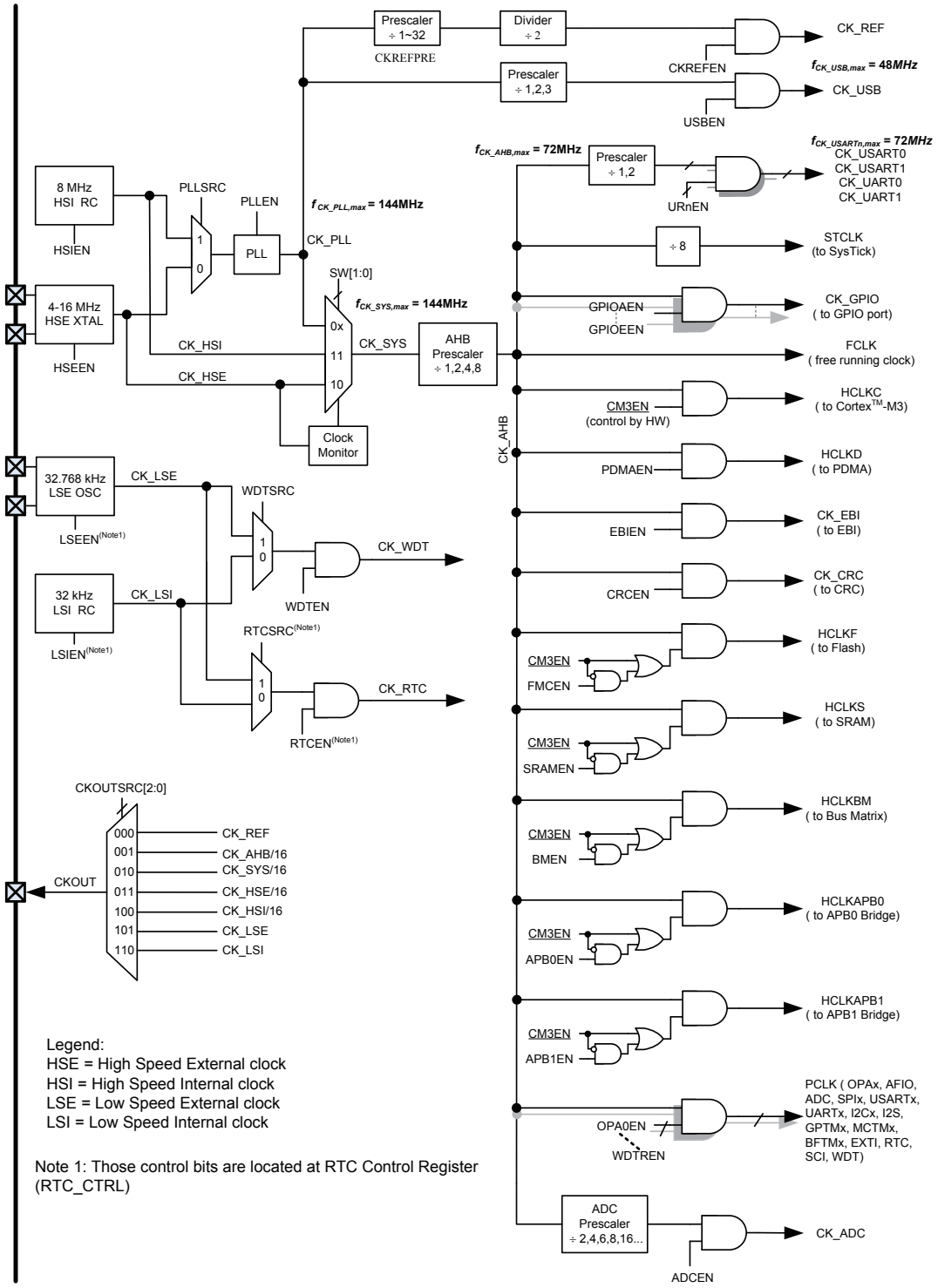


Figure 3. HT32F1656/1655 Clock Structure

Pin Assignment

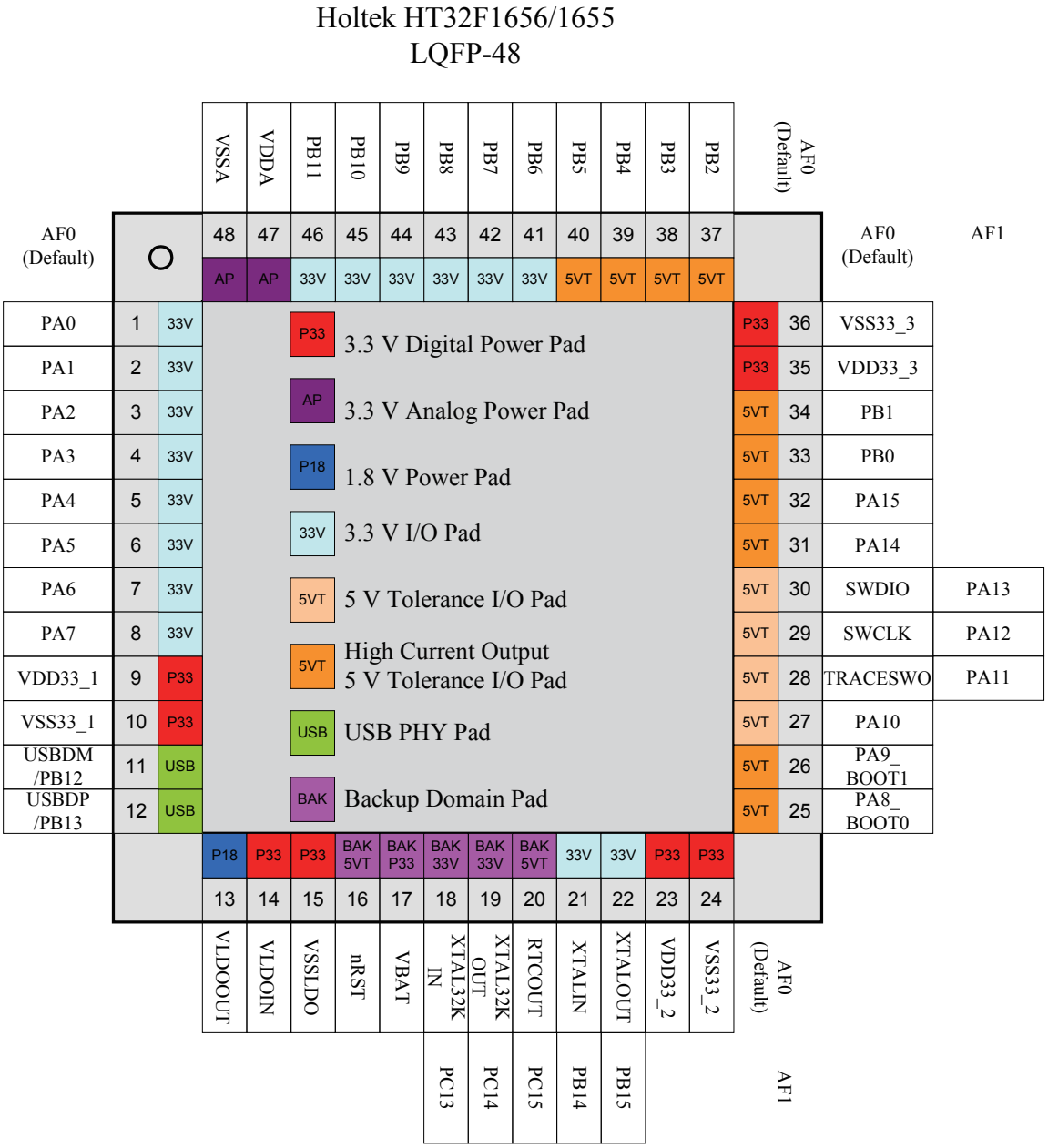


Figure 4. HT32F1656/1655 LQFP-48 Pin Assignment

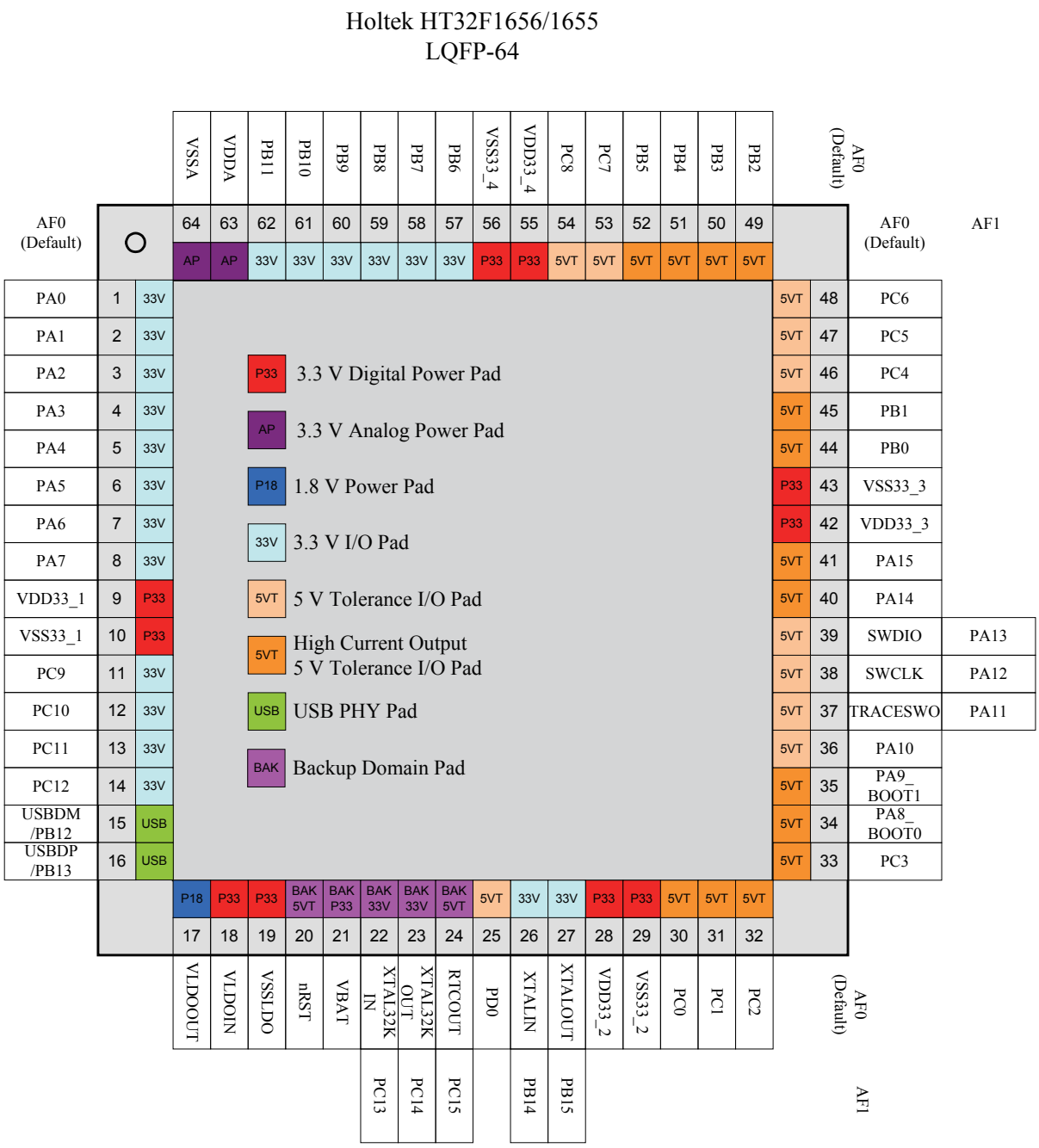


Figure 5. HT32F1656/1655 LQFP-64 Pin Assignment

Holtek HT32F1656/1655
LQFP-100

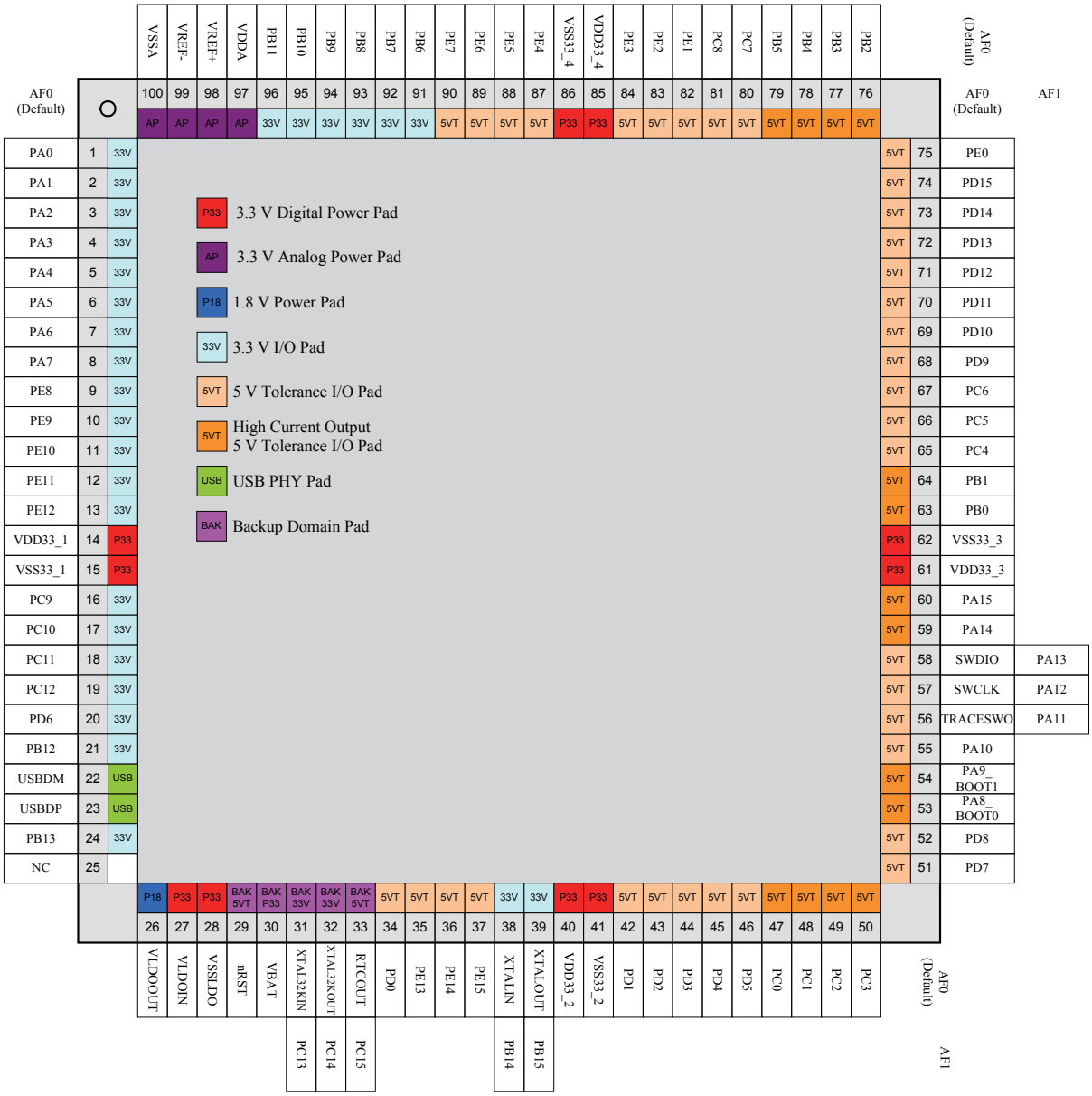


Figure 6. HT32F1656/1655 LQFP-100 Pin Assignment

Table 2. HT32F1656/55 Series Pin Assignment for LQFP100 / 64 / 48 Package

Package			Alternate function number														
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
LQFP-100	LQFP-64	LQFP-48	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I²C	SMC	EBI	I²S	N/A	N/A	N/A	N/A	System Other
1	1	1	PA0		ADC_IN0		GT1_CH0		USR0_RTS	I2C1_SCL	SCI_CLK		I2S_WS					
2	2	2	PA1		ADC_IN1		GT1_CH1		USR0_CTS	I2C1_SDA	SCI_DIO		I2S_ BCLK					
3	3	3	PA2		ADC_IN2		GT1_CH2		USR0_TX				I2S_ SDO					
4	4	4	PA3		ADC_IN3		GT1_CH3		USR0_RX				I2S_SDI					
5	5	5	PA4		ADC_IN4		GT0_CH0	SPI0_SCK	USR1_TX	I2C0_SCL								
6	6	6	PA5		ADC_IN5		GT0_CH1	SPI0_MOSI	USR1_RX	I2C0_SDA								
7	7	7	PA6		ADC_IN6		GT0_CH2	SPI0_MISO	USR1_RTS									
8	8	8	PA7		ADC_IN7		GT0_CH3	SPI0_SEL	USR1_CTS				I2S_ MCLK					
9			PE8		ADC_IN8			SPI1_SEL	USR0_RTS									
10			PE9		ADC_IN9			SPI1_SCK	USR0_CTS									
11			PE10		ADC_IN10			SPI1_MOSI	USR0_TX									
12			PE11		ADC_IN11			SPI1_MISO	USR0_RX									
13			PE12		ADC_IN12													
14	9	9	VDD33_1															
15	10	10	VSS33_1															
16	11		PC9		ADC_IN13		GT0_CH0	SPI1_SEL	UR0_TX	I2C1_SCL								
17	12		PC10		ADC_IN14		GT0_CH1	SPI1_SCK	UR0_RX	I2C1_SDA								
18	13		PC11		ADC_IN15		GT0_CH2	SPI1_MOSI										
19	14		PC12				GT0_CH3	SPI1_MISO										
20			PD6				GT0_ETI					EBI_ ARDY						
21	15	11	PB12				MT1_CH2			I2C0_SCL								
22	15	11	USBDM															
23	16	12	USBDP															
24	16	12	PB13				MT1_ CH2N			I2C0_SDA								
25			N.C.															
26	17	13	VLDOOUT															
27	18	14	VLDOIN															
28	19	15	VSSLDO															
29	20	16	nRST															
30	21	17	VBAT															
31	22	18	XTAL32KIN	PC13														
32	23	19	XTAL32KOUT	PC14														
33	24	20	RTCOUT	PC15_ WAKEUP														
34	25		PD0				MT1_ETI			I2C0_SDA		EBI_ A18	I2S_SDI					
35			PE13							I2C0_SCL		EBI_ A19	I2S_ MCLK					
36			PE14				GT1_ETI					EBI_ A20	I2S_WS					
37			PE15				GT1_CH0		UR0_TX			EBI_ A21						
38	26	21	XTALIN	PB14														
39	27	22	XTALOUT	PB15														
40	28	23	VDD33_2															

Package			Alternate function number														
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
LQFP-100	LQFP-64	LQFP-48	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I²C	SMC	EBI	I²S	N/A	N/A	N/A	N/A	System Other
41	29	24	VSS33_2															
42			PD1				GT1_CH1		UR0_RX			EBI_A22	I2S_BCLK					
43			PD2				GT1_CH2					EBI_A23	I2S_SDO					
44			PD3				GT1_CH3					EBI_A24	I2S_SDI					
45			PD4				MT1_CH0	SPI0_SEL		I2C1_SCL		EBI_A16	I2S_MCLK					
46			PD5				MT1_CH0N	SPI0_SCK		I2C1_SDA		EBI_A17						
47	30		PC0				GT1_CH0	SPI1_SEL				EBI_AD13	I2S_WS					
48	31		PC1				GT1_CH1	SPI1_SCK				EBI_AD14	I2S_BCLK					
49	32		PC2				GT1_CH2	SPI1_MOSI	UR1_TX	I2C0_SCL		EBI_AD15	I2S_SDO					
50	33		PC3				GT1_CH3	SPI1_MISO	UR1_RX	I2C0_SDA		EBI_CS3	I2S_SDI					
51			PD7							I2C1_SCL	SCI_CLK	EBI_A2						
52			PD8							I2C1_SDA	SCI_DIO	EBI_A0						
53	34	25	PA8_BOOT0						USR0_TX				I2S_MCLK					CKOUT
54	35	26	PA9_BOOT1					SPI0_MOSI				EBI_A1	I2S_WS					
55	36	27	PA10				MT1_CH1		USR0_RX		SCI_DET							
56	37	28	TRACESWO	PA11			MT1_CH1N	SPI0_MISO				EBI_A0	I2S_MCLK					TRACESWO
57	38	29	SWCLK	PA12														
58	39	30	SWDIO	PA13														
59	40	31	PA14				MT0_CH0	SPI1_SEL	USR1_TX		SCI_CLK	EBI_AD0						
60	41	32	PA15				MT0_CH0N	SPI1_SCK	USR1_RX		SCI_DIO	EBI_AD1						
61	42		VDD33_3															
62	43		VSS33_3															
63	44	33	PB0				MT0_CH1	SPI1_MOSI	USR0_TX	I2C0_SCL		EBI_AD2						
64	45	34	PB1				MT0_CH1N	SPI1_MISO	USR0_RX	I2C0_SDA		EBI_AD3						
65	46		PC4				MT1_CH2		USR1_RTS		SCI_CLK	EBI_AD10						
66	47		PC5				MT1_CH2N		USR1_CTS		SCI_DIO	EBI_AD11						
67	48		PC6				MT1_CH3				SCI_DET	EBI_AD12						
68			PD9					SPI0_SEL				EBI_A3						
69			PD10					SPI0_SCK				EBI_A4						
70			PD11					SPI0_MOSI				EBI_A5						
71			PD12					SPI0_MISO				EBI_A6						
72			PD13					SPI1_SEL				EBI_A7						
73			PD14					SPI1_SCK				EBI_A8						
74			PD15					SPI1_MOSI				EBI_A9						
75			PE0					SPI1_MISO				EBI_A10						
		35	VDD33_3															
		36	VSS33_3															
76	49	37	PB2				MT0_CH2	SPI0_SEL	UR0_TX			EBI_AD4						
77	50	38	PB3				MT0_CH2N	SPI0_SCK	UR0_RX			EBI_AD5						
78	51	39	PB4				MT0_BRK	SPI0_MOSI	UR1_TX			EBI_AD6						
79	52	40	PB5				MT1_BRK	SPI0_MISO	UR1_RX			EBI_AD7						

Package			Alternate function number														
			AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
LQFP -100	LQFP -64	LQFP -48	System Default	GPIO	ADC	CMP	MCTM /GPTM	SPI	USART /UART	I²C	SMC	EBI	I²S	N/A	N/A	N/A	N/A	System Other
80	53		PC7				MT0_CH3			I2C0_SCL		EBI_AD8						
81	54		PC8				MT0_ETI			I2C0_SDA		EBI_AD9						
82			PE1				MT1_CH0		USR1_TX		SCI_CLK	EBI_A11						
83			PE2				MT1_CH0N				SCI_DIO	EBI_A12						
84			PE3				MT1_CH1					EBI_A13						
85	55		VDD33_4															
86	56		VSS33_4															
87			PE4				MT1_CH1N			I2C1_SCL		EBI_A14						
88			PE5				MT1_CH2		USR1_RX	I2C1_SDA		EBI_A15						
89			PE6				MT1_CH2N		USR1_RTS			EBI_BL0	I2S_BCLK					
90			PE7				MT1_BRK		USR1_CTS			EBI_BL1	I2S_MCLK					
91	57	41	PB6			CN0	MT1_CH0	SPI1_SEL	UR1_TX			EBI_OE	I2S_MCLK					
92	58	42	PB7			CP0	MT1_CH0N	SPI1_SCK				EBI_CS0						
93	59	43	PB8			COUT0		SPI1_MOSI	UR1_RX			EBI_WE						
94	60	44	PB9			CN1	MT1_CH2	SPI1_MISO	UR0_TX			EBI_ALE	I2S_BCLK					
95	61	45	PB10			CP1	MT1_CH2N			I2C1_SCL		EBI_CS1	I2S_SDO					
96	62	46	PB11			COUT1	MT1_CH3		UR0_RX	I2C1_SDA		EBI_CS2	I2S_SDI					
97	63	47	VDDA															
98	63	47	VREF+															
99	64	48	VREF-															
100	64	48	VSSA															

Table 3. HT32F1656/55 Pin Description

Pin Number			Pin Name	Type (Note1)	IO Structure (Note2)	Output Driving	Description
LQFP 100	LQFP 64	LQFP 48					Default Function (AF0)
1	1	1	PA0	AI/O	33V	4/8mA	PA0
2	2	2	PA1	AI/O	33V	4/8mA	PA1
3	3	3	PA2	AI/O	33V	4/8mA	PA2
4	4	4	PA3	AI/O	33V	4/8mA	PA3
5	5	5	PA4	AI/O	33V	4/8mA	PA4
6	6	6	PA5	AI/O	33V	4/8mA	PA5
7	7	7	PA6	AI/O	33V	4/8mA	PA6
8	8	8	PA7	AI/O	33V	4/8mA	PA7
9		—	PE8	AI/O	33V	4/8mA	PE8
10		—	PE9	AI/O	33V	4/8mA	PE9
11		—	PE10	AI/O	33V	4/8mA	PE10
12		—	PE11	AI/O	33V	4/8mA	PE11
13			PE12	AI/O	33V	4/8mA	PE12
14	9	9	VDD33_1	P	—	—	3.3 V voltage for digital I/O
15	10	10	VSS33_1	P	—	—	Ground reference for digital I/O
16	11		PC9	AI/O	33V	4/8mA	PC9
17	12		PC10	AI/O	33V	4/8mA	PC10
18	13	—	PC11	AI/O	33V	4/8mA	PC11
19	14	—	PC12	I/O	33V	4/8mA	PC12
20			PD6	I/O	33V	4/8mA	PD6
21	15	11	PB12	I/O	5VT	8mA	PB12
22	15	11	USBDM	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
23	16	12	USBDP	AI/O	—	—	USB Differential data bus conforming to the Universal Serial Bus standard.
24	16	12	PB13	I/O	5VT	8mA	PB13
25			NC				No connection
26	17	13	VLDOOUT	P	—	—	LDO power 1.8 V output It is recommended to connect a capacitor, denoted as CLDO, as close as possible between this pin and VSSLDO.
27	18	14	VLDOIN	P	—	—	LDO power 3.3 V input Connected to the power switch circuitry for the internal backup domain.
28	19	15	VSSLDO	P	—	—	LDO ground reference
29	20	16	nRST	I(BK)	5VT_PU	—	External reset pin and external wakeup pin in the Power-Down mode
30	21	17	VBAT	P	—	—	Battery power input for the backup domain
31	22	18	PC13	AI/O (BK)	33V	1mA	XTAL32KIN
32	23	19	PC14	AI/O (BK)	33V	1mA	XTAL32KOUT
33	24	20	PC15	I/O (BK)	5VT	1mA	RTCOUT
34	25		PD0	I/O	5VT	8mA	PD0

Pin Number			Pin Name	Type (Note1)	IO Structure (Note2)	Output Driving	Description
LQFP 100	LQFP 64	LQFP 48					Default Function (AF0)
35			PE13	I/O	5VT	8mA	PE13
36			PE14	I/O	5VT	8mA	PE14
37			PE15	I/O	5VT	8mA	PE15
38	26	21	PB14	AI/O	33V	4/8mA	XTALIN
39	27	22	PB15	AI/O	33V	4/8mA	XTALOUT
40	28	23	VDD33_2	P	—	—	3.3 V voltage for digital I/O
41	29	24	VSS33_2	P	—	—	Ground reference for digital I/O
42			PD1	I/O	5VT	8mA	PD1
43			PD2	I/O	5VT	8mA	PD2
44			PD3	I/O	5VT	8mA	PD3
45			PD4	I/O	5VT	8mA	PD4
46			PD5	I/O	5VT	8mA	PD5
47	30		PC0	I/O	5VT	12mA	PC0
48	31		PC1	I/O	5VT	12mA	PC1
49	32		PC2	I/O	5VT	12mA	PC2
50	33		PC3	I/O	5VT	12mA	PC3
51			PD7	I/O	5VT	8mA	PD7
52			PD8	I/O	5VT	8mA	PD8
53	34	25	PA8	I/O	5VT_PU	12mA	PA8
54	35	26	PA9	I/O	5VT_PU	12mA	PA9
55	36	27	PA10	I/O	5VT	8mA	PA10
56	37	28	PA11	I/O	5VT	8mA	TRACESWO
57	38	29	PA12	I/O	5VT_PU	8mA	SWCLK
58	39	30	PA13	I/O	5VT_PU	8mA	SWDIO
59	40	31	PA14	I/O	5VT_PU	12mA	PA14
60	41	32	PA15	I/O	5VT_PU	12mA	PA15
61	42		VDD33_3	P	—	—	3.3 V voltage for digital I/O
62	43		VSS33_3	P	—	—	Ground reference for digital I/O
63	44	33	PB0	I/O	5VT	12mA	PB0
64	45	34	PB1	I/O	5VT	12mA	PB1
65	46		PC4	I/O	5VT	8mA	PC4
66	47		PC5	I/O	5VT	8mA	PC5
67	48		PC6	I/O	5VT	8mA	PC6
68			PD9	I/O	5VT	8mA	PD9
69			PD10	I/O	5VT	8mA	PD10
70			PD11	I/O	5VT	8mA	PD11
71			PD12	I/O	5VT	8mA	PD12
72			PD13	I/O	5VT	8mA	PD13
73			PD14	I/O	5VT	8mA	PD14
74			PD15	I/O	5VT	8mA	PD15
75			PE0	I/O	5VT	8mA	PE0

Pin Number			Pin Name	Type (Note1)	IO Structure (Note2)	Output Driving	Description
LQFP 100	LQFP 64	LQFP 48					Default Function (AF0)
		35	VDD33_3	P	—	—	3.3 V voltage for digital I/O
		36	VSS33_3	P	—	—	Ground reference for digital I/O
76	49	37	PB2	I/O	5VT	12mA	PB2
77	50	38	PB3	I/O	5VT	12mA	PB3
78	51	39	PB4	I/O	5VT	12mA	PB4
79	52	40	PB5	I/O	5VT	12mA	PB5
80	53		PC7	I/O	5VT	8mA	PC7
81	54		PC8	I/O	5VT	8mA	PC8
82			PE1	I/O	5VT	8mA	PE1
83			PE2	I/O	5VT	8mA	PE2
84			PE3	I/O	5VT	8mA	PE3
85	55		VDD33_4	P	—	—	3.3 V voltage for digital I/O
86	56		VSS33_4	P	—	—	Ground reference for digital I/O
87			PE4	I/O	5VT	8mA	PE4
88			PE5	I/O	5VT	8mA	PE5
89			PE6	I/O	5VT	8mA	PE6
90			PE7	I/O	5VT	8mA	PE7
91	57	41	PB6	AI/O	33V	4/8mA	PB6
92	58	42	PB7	AI/O	33V	4/8mA	PB7
93	59	43	PB8	AI/O	33V	4/8mA	PB8
94	60	44	PB9	AI/O	33V	4/8mA	PB9
95	61	45	PB10	AI/O	33V	4/8mA	PB10
96	62	46	PB11	AI/O	33V	4/8mA	PB11
97	63	47	VDDA	P	—	—	3.3 V analog voltage for ADC and OPA/ Comparator
98			VREF+	P	—	—	ADC positive reference voltage has to be lower or equal to VDDA
99			VREF-	P	—	—	ADC negative reference voltage has to be directly connected to VSSA
100	64	48	VSSA	P	—	—	Ground reference for the ADC and OPA/ Comparator

Note: 1. I = Input, O = Output, A = Analog port, P = Power supply, PU = Pull-up, BK = Back-up domain

2. 5VT = 5 V tolerant; 33V = 3.3 V tolerant.

3. The GPIOs are in an AF0 state after a V_{DD18} power on reset (POR) except for the RTCOUT pin in the Backup Domain I/O. The RTCOUT pin is reset by the Backup Domain power-on-reset (PORB) or by the Backup Domain software reset (BAK_RST bit in BAK_CR register).

4. The backup domain of the I/O pins have a source current capability limitation of $< 1mA$ @ $V_{BAT} = 3.3V$.

4 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD33}	External main supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{LDOIN}	External LDO supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5 V-tolerant I/O	V_{SS} - 0.3	V_{SS} + 5.5	V
	Input voltage on other I/O	V_{SS} - 0.3	V_{DD33} + 0.3	V
T_A	Ambient operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C
P_D	Total power dissipation	—	500	mW
V_{ESD}	Electrostatic discharge voltage - human body mode	-4000	+4000	V

Recommended DC Operating Conditions

Table 5. Recommended DC Operating Conditions

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	I/O operating voltage	—	2.7	3.3	3.6	V
V_{DDA}	Analog operating voltage	—	2.7	3.3	3.6	V
V_{BAT}	Battery supply operating voltage	—	2.7	3.3	3.6	V
V_{LDOIN}	LDO operating voltage	—	2.7	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 6. LDO Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LDOOUT}	Internal regulator output voltage	V_{LDOIN} = 3.3V Regulator input	1.71	1.8	1.89	V
I_{LDOOUT}	Output current	V_{LDOIN} = 2.7V Regulator input	—	—	200	mA
C_{LDO}	External filter capacitor value for internal core power supply	The capacitor value is dependent on the core power current consumption	2.2	—	10	μF

Power Consumption

Table 7. Power Consumption Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD33} = V_{BAT} = 3.3 V, HSE = 8MHz, PLL = 144MHz, f_{HCLK} = 72MHz, f_{PCLK} = 72MHz, All peripherals enabled	—	62	72	mA
		V_{DD33} = V_{BAT} = 3.3 V, HSE = 8MHz, PLL = 144MHz, f_{HCLK} = 72MHz, f_{PCLK} = 72MHz, All peripherals disabled	—	29	34	mA
	Supply current (Sleep mode)	V_{DD33} = V_{BAT} = 3.3 V, HSE = 8MHz, PLL = 144 MHz, f_{HCLK} = 0MHz, f_{PCLK} = 72MHz, All peripherals enabled	—	43	50	mA
		V_{DD33} = V_{BAT} = 3.3 V, HSE = 8MHz, PLL = 144MHz, f_{HCLK} = 0MHz, f_{PCLK} = 72MHz, All peripherals disabled	—	8.5	12	mA
	Supply current (Deep-Sleep1 mode)	V_{DD33} = V_{BAT} = 3.3 V, All clock off (HSE/PLL/f_{HCLK}), LDO in low power mode, LSI on, RTC on	—	63	90	μA
	Supply current (Deep-Sleep2 mode)	V_{DD33} = V_{BAT} = 3.3 V, All clock off (HSE/PLL/f_{HCLK}), LDO off (DMOS on), LSI on, RTC on	—	20	25	μA
	Supply current (Power-Down mode)	V_{DD33} = V_{BAT} = 3.3 V, LDO off, LSE on, LSI off, RTC on	—	—	—	μA
		V_{DD33} = V_{BAT} = 3.3 V, LDO off, LSE on, LSI off, RTC off	—	—	—	μA
		V_{DD33} = V_{BAT} = 3.3 V, LDO off, LSE off, LSI on, RTC on	—	—	—	μA
		V_{DD33} = V_{BAT} = 3.3 V, LDO off, LSE off, LSI on, RTC off	—	5	6	μA
I_{BAT}	Battery supply current (Power-Down mode)	V_{DD33} not present, V_{BAT} = 3.3 V, LDO off, LSE off, LSI on, RTC on	—	4	—	μA
		V_{DD33} not present, V_{BAT} = 3.3 V, LDO off, LSE off, LSI on, RTC off	—	3.9	—	μA

Note: 1. HSE means high speed external oscillator. HSI means 8MHz high speed internal oscillator.
2. LSE means low speed external oscillator. LSI means 32.768KHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 8. LVD/BOD Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOD}	Brown Out Detector Voltage	—	—	2.6	—	V
V_{LVD}	Voltage of Low Voltage Detector	LVDS (Note1) = '000'	—	2.7	—	V
		LVDS (Note1) = '001'	—	2.8	—	V
		LVDS (Note1) = '010'	—	2.9	—	V
		LVDS (Note1) = '011'	—	3.0	—	V
		LVDS (Note1) = '100'	—	3.1	—	V
		LVDS (Note1) = '101'	—	3.2	—	V
		LVDS (Note1) = '110'	—	3.4	—	V
		LVDS (Note1) = '111'	—	3.5	—	V
V_{POR}	Power On Reset Voltage	—	—	1.36	—	V

Note: LVDS field is in PWRCU LVDCSR register

External Clock Characteristics

Table 9. High Speed External Clock (HSE) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High Speed External oscillator frequency (HSE)	V_{DD33} = 3.3 V	4	—	16	MHz
C_{HSE}	Recommended load capacitance on XTALIN and XTALOUT pins		—	TBD	—	pF
R_{FHSE}	Recommended external feedback resistor between XTALIN and XTALOUT pins		—	1.0	—	MΩ
D_{HSE}	HSE oscillator Duty cycle		40	—	60	%
I_{DDHSE}	HSE oscillator current consumption	V_{DD33} = 3.3 V, T_A = 25°C	—	0.96	—	mA
I_{STBHSE}	HSE oscillator standby current	V_{DD33} = 3.3 V, T_A = 25°C	—	—	0.1	μA
t_{SUHSE}	HSE oscillator startup time	V_{DD33} = 3.3 V, T_A = 25°C	—	—	4	ms

Table 10. Low Speed External Clock (LSE) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low Speed External oscillator frequency (LSE)	$V_{DD33} = V_{BAT}$ = 3.3 V	—	32.768	—	kHz
C_{LSE}	Recommended load capacitance on XTAL32KIN and XTAL32KOUT pins		—	TBD	—	pF
R_{FLSE}	Recommended external feedback resistor between XTAL32KIN and XTAL32KOUT pins		—	10	—	MΩ
D_{LSE}	LSE oscillator Duty cycle		40	—	60	%
I_{DDLSE}	LSE Oscillator Operating current	$V_{DD33} = V_{BAT}$ = 3.3 V, LSESM = 0 (Normal startup mode)	—	1.7	—	μA
I_{STBLSE}	LSE Oscillator Standby current	$V_{DD33} = V_{BAT}$ = 3.3 V, LSESM = 1 (Fast startup mode)	—	3	8	μA
t_{SULSE}	LSE Oscillator Startup time	$V_{DD33} = V_{BAT}$ = 3.3 V, LSESM = 1 (Fast startup mode)	—	200	—	ms

Note: The following PCB layout guidelines are recommended to increase the stability of the crystal circuit for the HSE/LSE clock:

1. The crystal oscillator should be located as close as possible to the MCU to minimise trace length thus reducing parasitic capacitance.
2. Use a ground plane as a shield under the crystal circuit to reduce the effects of noise interference.
3. Route high frequency signals away from crystal oscillator area to prevent crosstalk.

Internal Clock Characteristics

Table 11. High Speed Internal Clock (HSI) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	High Speed Internal Oscillator Frequency (HSI)	V_{DD33} = 3.3 V, T_A = -40°C ~ +85°C	—	8	—	MHz
ACC_{HSI}	HSI Oscillator Frequency accuracy	Factory-trimmed, V_{DD33} = 3.3 V, T_A = -40°C ~+85°C	-5	—	+5	%
D_{HSI}	HSI Oscillator Duty cycle	V_{DD33} = 3.3 V, f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	HSI Oscillator current	V_{DD33} = 3.3 V, f_{HSI} = 8 MHz	—	0.92	—	mA
t_{SUHSI}	HSI Oscillator Startup time	V_{DD33} = 3.3 V, f_{HSI} = 8 MHz, HSIRCBL = 0 (HSI Ready Counter Bits Length 7 Bits)	—	17	—	μs

Note: HSIRCBL field is in PWRCU HSIRCR register

Table 12. Low Speed Internal Clock (LSI) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	$V_{DD33} = V_{BAT}$ = 3.3 V, T_A = -40°C ~ +85°C	25	32	43	kHz
I_{DDLSI}	LSI Oscillator Operating current	$V_{DD33} = V_{BAT}$ = 3.3 V, T_A = 25°C	—	1.0	2	μA
t_{SULSI}	LSI Oscillator startup time	$V_{DD33} = V_{BAT}$ = 3.3 V, T_A = 25°C	—	35	—	ms

PLL Characteristics

Table 13. PLL Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock		4	—	16	MHz
f_{CK_PLL}	PLL output clock		8	—	144	MHz
t_{LOCK}	PLL lock time		—	TBD	—	ms

Memory Characteristics

Table 14. Flash Memory Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{ENDU}	Number of guaranteed program/erase cycles before failure. (Endurance)	T_A = -40°C ~ +85°C	20	—	—	K cycles
T_{RET}	Data retention time	T_A = 25°C	100	—	—	Years
t_{PROG}	Word programming time	T_A = -40°C ~ +85°C	20	—	40	μs
t_{ERASE}	Page erase time	T_A = -40°C ~ +85°C	20	—	40	ms
t_{MERASE}	Mass erase time	T_A = -40°C ~ +85°C	20	—	40	ms

I/O Port Characteristics

Table 15. I/O Port Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IL}	Low level input current	3.3 V IO	V_I = 0 V, On-chip pull-up resister disabled.	—	—	3	μA
		5 V-tolerant IO		—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High level input current	3.3 V IO	V_I = V_{DD33}, On-chip pull-down resister disabled.	—	—	3	μA
		5 V-tolerant IO		—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low level input voltage	3.3 V IO		-0.3	—	0.8	V
		5 V-tolerant IO		-0.3	—	0.8	V
		Reset pin		-0.3	—	0.8	V
V_{IH}	High level input voltage	3.3 V IO		2	—	3.6	V
		5 V-tolerant IO		2	—	5.5	V
		Reset pin		2	—	5.5	V
V_{HYS}	Schmitt trigger input voltage hysteresis	3.3 V IO		—	400	—	mV
		5 V-tolerant IO		—	400	—	mV
		Reset pin		—	400	—	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OL}	Low level output current (GPIO Sink current)	3.3 V IO 4 mA drive, V_{OL} = 0.4 V	4	—	—	mA
		3.3 V IO 8 mA drive, V_{OL} = 0.4 V	8	—	—	mA
		5 V-tolerant IO 8 mA drive, V_{OL} = 0.4 V	8	—	—	mA
		5 V-tolerant IO 12 mA drive, V_{OL} = 0.4 V	12	—	—	mA
		Backup Domain IO drive @ V_{BAT} = 3.3 V, V_{OL} = 0.4 V, PC13, PC14, PC15	—	4	—	mA
I_{OH}	High level output current (GPIO Source current)	3.3 V I/O 4 mA drive, V_{OH} = V_{DD33} - 0.4 V	4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OH} = V_{DD33} - 0.4 V	8	—	—	mA
		5 V-tolerant I/O 8 mA drive, V_{OH} = V_{DD33} - 0.4 V	8	—	—	mA
		5 V-tolerant I/O 12 mA drive, V_{OH} = V_{DD33} - 0.4 V	12	—	—	mA
		Backup Domain IO drive @ V_{BAT} = 3.3 V, V_{OL} = V_{DD33} - 0.4 V, PC13, PC14, PC15	—	—	1	mA
V_{OL}	Low level output voltage	3.3 V 4 mA drive IO, I_{OL} = 4 mA	—	—	0.4	V
		3.3 V 8 mA drive IO, I_{OL} = 8 mA	—	—	0.4	V
		5 V-tolerant 8 mA drive IO, I_{OL} = 8 mA	—	—	0.4	V
		5 V-tolerant 12 mA drive IO, I_{OL} = 12 mA	—	—	0.4	V
V_{OH}	High level output voltage	3.3 V 4 mA drive IO, I_{OH} = 4 mA	V_{DD33} - 0.4 V	—	—	V
		3.3 V 8 mA drive IO, I_{OH} = 8 mA	V_{DD33} - 0.4 V	—	—	V
		5 V-tolerant 8 mA drive IO, I_{OH} = 8 mA	V_{DD33} - 0.4 V	—	—	V
		5 V-tolerant 12 mA drive IO, I_{OH} = 12 mA	V_{DD33} - 0.4 V	—	—	V
R_{PU}	Internal pull-up resistor	3.3 V I/O	34		74	kΩ
		5 V-tolerant I/O	38		89	kΩ
R_{PD}	Internal pull-down resistor	3.3 V I/O	29		86	kΩ
		5 V-tolerant I/O	35		107	kΩ

ADC Characteristics

Table 16. ADC Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.7	3.3	3.6	V
V_{ADCIN}	A/D Converter input voltage range		0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference voltage			V_{DDA}	V_{DDA}	V
I_{ADC}	Current consumption	V_{DDA} = 3.3 V	—	1	TBD	mA
I_{ADC_DN}	Power down current consumption	V_{DDA} = 3.3 V	—	1	10	μA
f_{ADC}	A/D Converter clock		0.7	—	14	MHz
f_S	Sampling rate		0.05	—	1	MHz
$f_{ADCCONV}$	A/D Converter conversion time		—	14	—	$1/f_{ADC}$ Cycles
R_I	Input sampling switch resistance		—	—	1	kΩ
C_I	Input sampling capacitance	No pin/pad capacitance included	—	—	5	pF
t_{SU}	Startup up time		—	—	1	μs
N	Resolution		—	12	—	bits
INL	Integral Non-linearity error	f_S = 1 MHz, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-linearity error	f_S = 1 MHz, V_{DDA} = 3.3 V	—	—	±1	LSB
E_O	Offset error		—	—	±10	LSB
E_G	Gain error		—	—	±10	LSB

Note: 1. Guaranteed by design, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $1.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S may not have an arbitrarily large value.

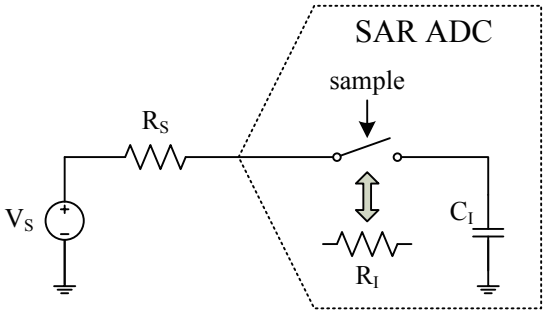


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0V and VREF) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{1.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, Rs may be larger than the value indicated by the equation above.

Operational Amplifier/Comparator Characteristics

Table 17. OPA/CMP Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage		2.7	3.3	3.6	V
$I_{OPA/CMP}$	Typical operating current		—	230	—	μA
I_{OPA/CMP_DN}	Power down supply current	Assign registers OPAEN = 0 and EN_OPAOP = 0	—	—	0.1	μA
V_{IOS}	Input offset voltage	V_{DDA} = 3.3 V, AnOF[5:0] = '100000'	-15	—	15	mV
		V_{DDA} = 3.3 V, After calibration	-1	—	1	mV
V_{IOS_DRIFT}	Input offset voltage drift	T_A = -40°C ~ +85°C			0.04	mV/°C
R_{INPUT}	Input resistance			10		MΩ
GV	Voltage Gain		60	100		dB
U_t	Unit-Gain Bandwidth	R_L=100KΩ		1,3		MHz
		R_L=100KΩ, C_L=100pF		1.24		
V_{CM}	OPA common mode voltage range	V_{DDA} = 3.3 V	V_{SSA}	—	V_{DDA} – 1.2	V
V_{OV}	OPA output voltage swing	V_{DDA} = 3.3 V	V_{SSA} + 0.3		V_{DDA} – 0.5	V
SR	Slew Rate	V_{DDA} = 3.3 V; Output capacitor load C_L=100pF		1.6		V/μs
t_{RT}	Comparator response time	V_{DDA} = 3.3 V; Input Overdrive = ±10mV	—	1	—	μs

Note: Guaranteed by design, not tested in production.

GPTM/MCTM Characteristics

Table 18. GPTM/MCTM Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TM}	Timer clock source for GPTM and MCTM	—	—	—	72	MHz
t_{RES}	Timer resolution time	—	1	—	—	f_{TM}
f_{EXT}	External single frequency on channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer resolution	—	—	—	16	bits

I²C Characteristics

Table 19. I²C Characteristics

Symbol	Parameter	Standard mode		Fast mode		Fast mode plus		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	—	100		400		1000	kHz
$t_{SCL(H)}$	SCL clock high time	4.5		1.125		0.45		μs
$t_{SCL(L)}$	SCL clock low time	4.5		1.125		0.45		μs
t_{FALL}	SCL and SDA fall time		1.3		0.34		0.135	μs
t_{RISE}	SCL and SDA rise time		1.3		0.34		0.135	μs
$t_{SU(SDA)}$	SDA data setup time	500		125		50		ns
$t_{H(SDA)}$	SDA data hold time	0		0		0		ns
$t_{SU(STA)}$	START condition setup time	500		125		50		ns
$t_{H(STA)}$	START condition hold time	0		0		0		ns
$t_{SU(STO)}$	STOP condition setup time	500		125		50		ns

Note: 1. Guaranteed by design, not tested in production.
2. To achieve 100kHz standard mode, the peripheral clock frequency must be higher than 2MHz.
3. To achieve 400kHz fast mode, the peripheral clock frequency must be higher than 8MHz.
4. To achieve 1MHz fast mode plus, the peripheral clock frequency must be higher than 20MHz.
5. The above characteristic parameters of the I²C bus timing are based on: SEQ_FILTER = 01 and COMB_FILTER_En is disabled.

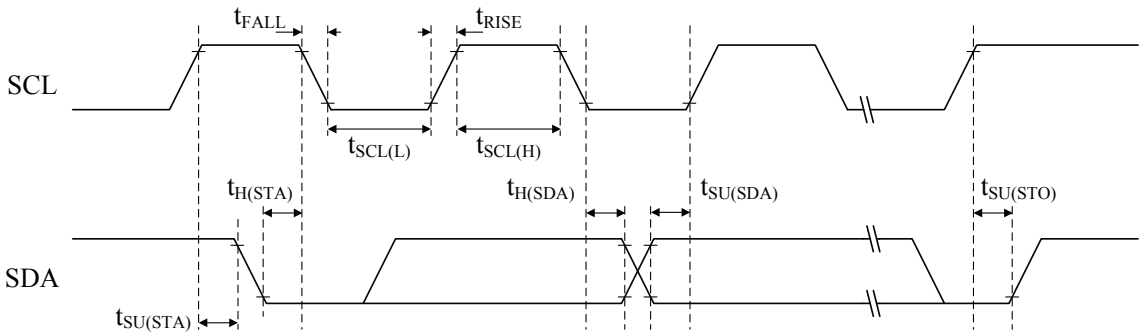


Figure 8. I²C Timing Diagrams

SPI Characteristics

Table 20. SPI Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency		—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$	SCK clock high time		$f_{PCLK}/8$	—	—	ns
$t_{SCK(L)}$	SCK clock low time		$f_{PCLK}/8$	—	—	ns
SPI Master mode						
$t_{V(MO)}$	Data output valid time		—	—	5	ns
$t_{H(MO)}$	Data output hold time		2	—	—	ns
$t_{SU(MI)}$	Data input setup time		5	—	—	ns
$t_{H(MI)}$	Data input hold time		5	—	—	ns
SPI Slave mode						
$t_{SU(SEL)}$	SEL enable setup time		4 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL enable hold time		2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data output access time		—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data output disable time		—	—	10	ns
$t_{V(SO)}$	Data output valid time		—	—	25	ns
$t_{H(SO)}$	Data output hold time		15	—	—	ns
$t_{SU(SI)}$	Data input setup time		5	—	—	ns
$t_{H(SI)}$	Data input hold time		4	—	—	ns

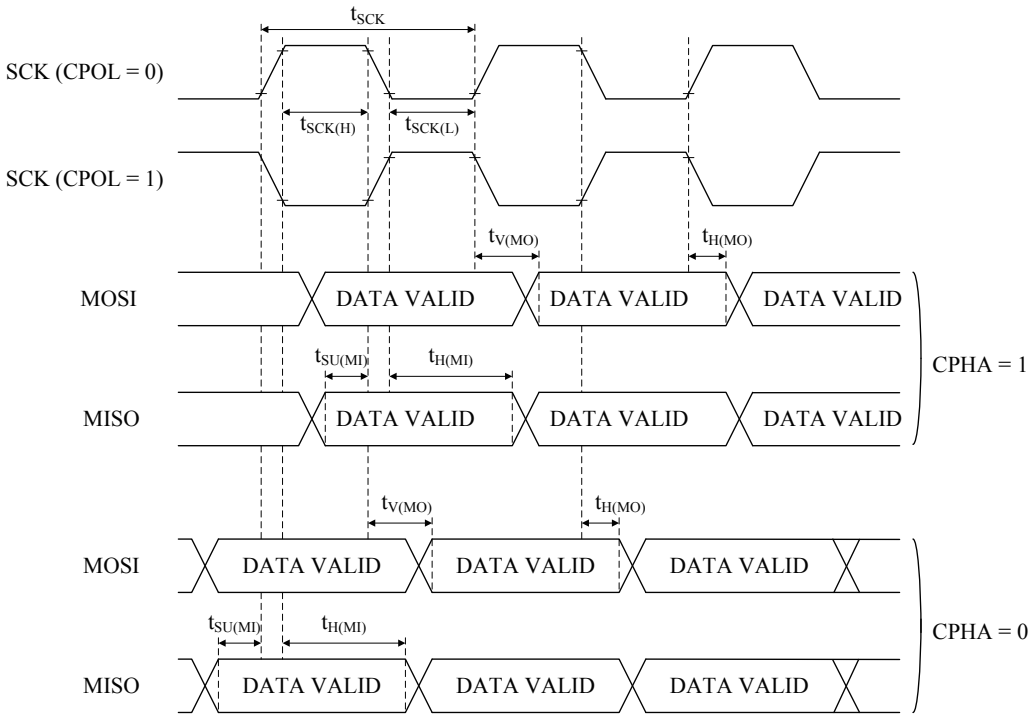


Figure 9. SPI Timing Diagrams - SPI Master Mode

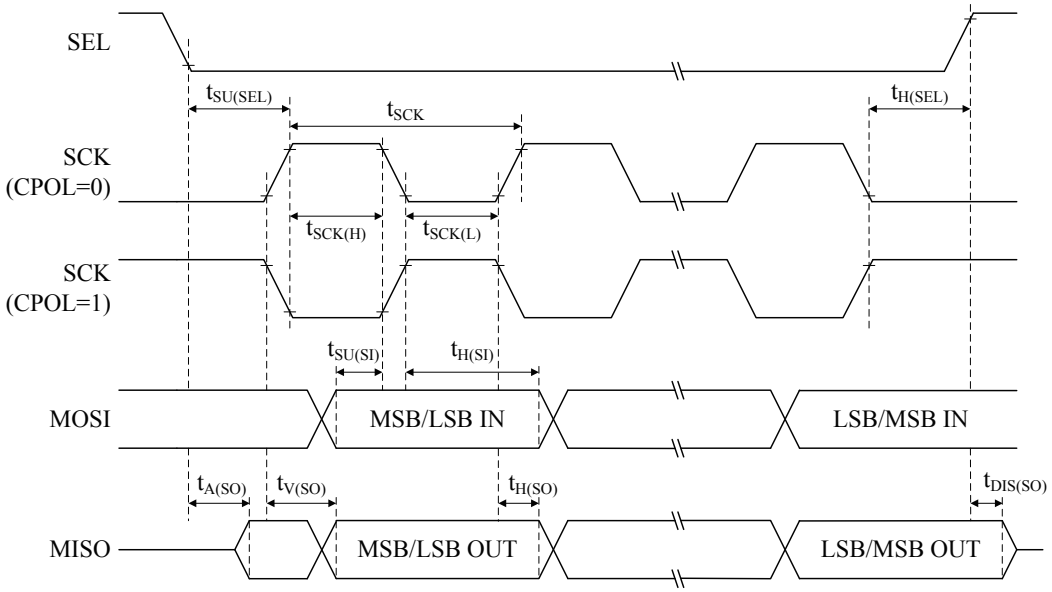


Figure 10. SPI Timing Diagrams - SPI Slave Mode with CPHA=1

I²S Characteristics

Table 21. I²S Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²S Master mode						
$t_{WSD(MO)}$	WS output to BCLK delay			TBD		ns
$t_{DOD(MO)}$	Data output to BCLK delay			TBD		ns
$t_{DIS(MI)}$	Data input setup time			TBD		ns
$t_{DIH(MI)}$	Data input hold time			TBD		ns
I²S Slave mode						
$t_{BCH(SI)}$	BCLK high pulse width			TBD		ns
$t_{BCL(SI)}$	BCLK low pulse width			TBD		ns
$t_{WSS(SI)}$	WS input setup time			TBD		ns
$t_{DOD(SO)}$	Data output to BCLK delay			TBD		ns
$t_{DIS(SI)}$	Data input setup time			TBD		ns
$t_{DIH(SI)}$	Data input hold time			TBD		ns

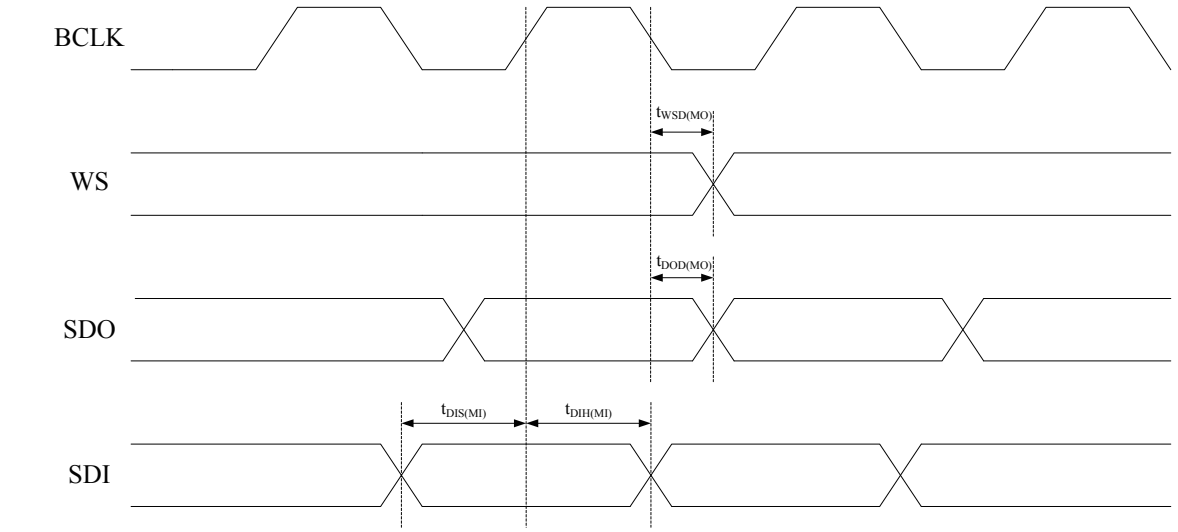


Figure 11. Timing of I²S Master Mode

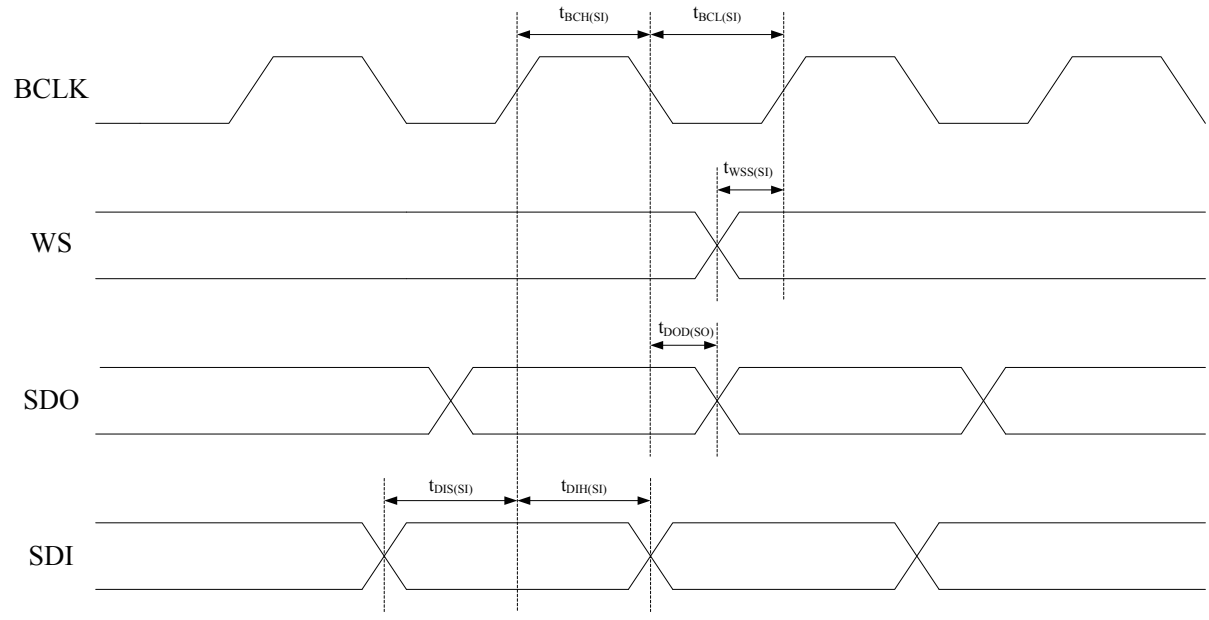


Figure 12. Timing of I²S Slave Mode

USB Characteristics

The USB interface is USB-IF certified – Full Speed.

Table 22. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	USB operating voltage		3.0	—	3.6	V
V_{DI}	Differential input sensitivity	|USBDP-USBDM|	0.2	—	—	V
V_{CM}	Common mode voltage range		0.8	—	2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
V_{OL}	Pad output low voltage	R_L of 1.5kΩ to V_{DD33}	0	—	0.3	V
V_{OH}	Pad output high voltage		2.8	—	3.6	V
V_{CRS}	Differential output signal cross-point voltage		1.3		2.0	V
Z_{DRV}	Driver output resistance		—	10	—	Ω
C_{IN}	Transceiver pad capacitance			—	20	pF

Note: 1. Guaranteed by design, not tested in production.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP pin should be pulled up with a 1.5kΩ external resistor to a 3.0-to-3.6 V voltage supply.
3. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which will experience degradation in the 2.7-to-3.0 V V_{DD33} voltage range.
4. RL is the load connected to the USB driver USBDP.

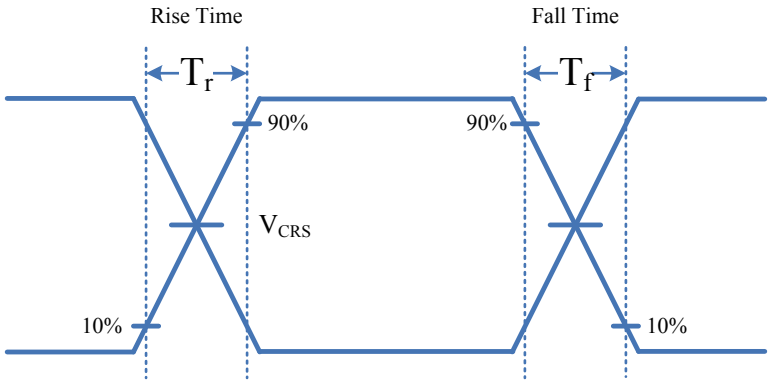


Figure 13. USB Signal Rise Time and Fall time and Cross-Point Voltage (V_{CRS}) Definition

Table 23 USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_r	Rise time	C_L = 50 pF	4	—	20	ns
T_f	Fall time	C_L = 50 pF	4	—	20	ns
$T_{r/f}$	Rise time / fall time matching	$T_{r/f} = T_r / T_f$	90	—	110	%

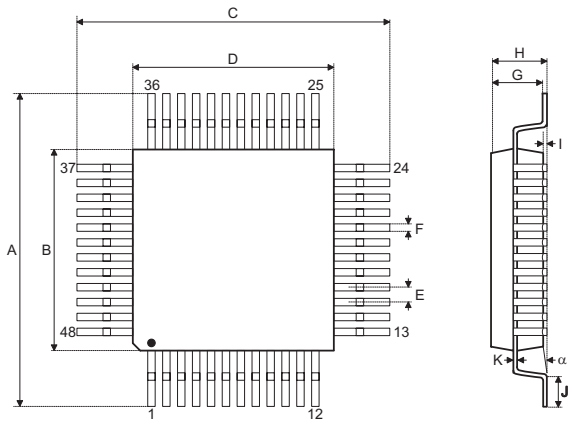
5 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

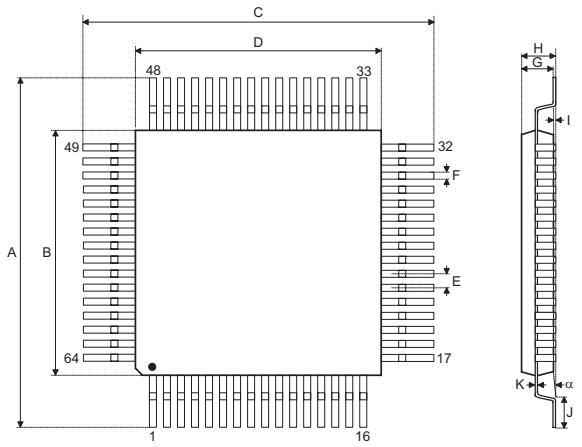
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.0 BSC	—
B	—	7.0 BSC	—
C	—	9.0 BSC	—
D	—	7.0 BSC	—
E	—	0.5 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

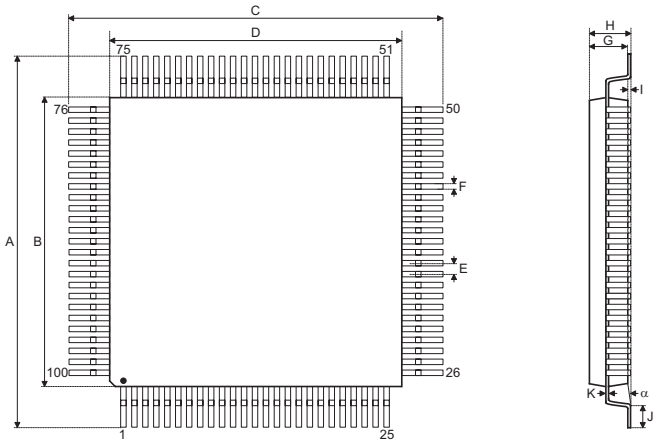
64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

100-pin LQFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.630 BSC	—
B	—	0.551 BSC	—
C	—	0.630 BSC	—
D	—	0.551 BSC	—
E	—	0.020 BSC	—
F	0.007	0.009	0.011
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	16.00 BSC	—
B	—	14.00 BSC	—
C	—	16.00 BSC	—
D	—	14.00 BSC	—
E	—	0.50 BSC	—
F	0.17	0.22	0.27
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°